REMARKS

Reconsideration and withdrawal of the outstanding objection to the drawings and rejection of claims, in view of this submission, is respectfully requested.

By the above-made amendments, claims 1 and 3-31 are now pending of which claims 1, 3, 8-9, 11-12, 14-15, and 18-19 were amended, claim 2 was cancelled and claims 21-31 were newly presented. The amendments made to the claims are in consideration of effecting further clarification of the subject matter being covered thereby and include changes for purposes of highlighting the various inventive aspects thereof over that previously known including over the art documents applied in the outstanding rejections. With regard to claims 3 and 11, revisions were implemented therein in consideration of effecting clarification regarding the questioned set forth limitations thereof and thereby obviating the outstanding objection to the drawings, under item 1 on page 2 of the Office Action. The newly-added dependent claims 21-31 particularly highlight various structural aspects relating to the electrically insulating layer (e.g., layer 5) and other component elements of the device and with regard to the relative positional placement thereof.

With regard to independent claim 1, the further limiting aspects included in original dependent claim 2 (now cancelled) are now incorporated therein. Namely, the originally set forth expression "a semiconductor element" now reads as "a semiconductor element formed in a surface of the wafer including a transistor portion." This can be seen with regard to wafer 9 which includes a transistor portion 110 shown in Fig. 20 of the drawings, although not limited

thereto. The further limiting aspect in the second "wherein" clause of original claim 2, also, is now included in independent claim 1 in connection with the expression "the transistor portion is covered with a portion of the electrically insulating layer". This can be seen in the drawings with regard to stress relaxation layer 5 such as shown in Figs. 20, 21, et seq., although not limited thereto. The invention according to independent claim 1 further sets forth the particularities of the external connection terminal and the electrically insulating layer including the positioning thereof as it relates to the covering of the transistor portion (e.g., 110) including the thickness thereof. Supportive discussion regarding the set forth electrically insulating layer and its placement in relation to the other component elements of the semiconductor device according to independent claim 1 is given on page 58, line 18, to page 62, line 2, of the present specification; and Figs. 19-21 and 38, etc., although not limited thereto. Similar featured aspects as that contained in independent claim 1 are contained also with regard to independent claims 3, 11, 14, and 18, although presented somewhat differently therefrom.

Regarding the further limiting aspect according to the now-amended independent claim 3, the invention calls for, among the various featured aspects thereof, "the transistor portion [to be] placed in an outer circumferential portion of the surface of the semiconductor device with respect to the at least one electrode," and "the transistor portion is covered with a portion of the electrically insulating layer having a thickness in the range of from 35 to 150 micrometers." Supportive discussion regarding this is found, for example, from page 60, line

11, to page 62, line 2, of the present specification and Figs. 21, 38 and 39, although not limited thereto.

As discussed in the specification, in the case the stress relaxation layer (e.g., layer 5) is formed in an area that is hardly affected by α-rays, the thickness thereof may be made smaller than 35 micrometers (e.g., see the relatively thin stress insulating layer 5 portion beneath the rightmost solder bump shown in Fig. 21 of the drawings.) Further, as a portion of the electrically insulating layer approaches the outer circumference of the semiconductor device, the portion is apt to suffer strain with induced thermal stress. Hence, the stress relaxation layer is required to be made thicker at that portion. It is thus preferable that a transistor area of the wafer that is apt to be easily affected by α-rays is disposed in the outer circumference of the semiconductor device whereas the area that is not so affected by α-rays is disposed in the more centrally located position on the device, with respect to a plan view of the surface thereof. This can be seen with regard to Fig. 38 of the drawings and from the related discussion beginning on page 60, line 11, et seq. of the present specification. The discussion therein is also applicable with regard to amended claim 1.

Incidentally, the referred to "second portion" of the electrically insulating layer can be seen with regard to the portion of stress relaxation layer 5 having the incline such as at the edge thereof. Regarding the semiconductor device according to claims 1 and 3-31, as currently amended, the "external connection terminal" can be seen with regard to reference numeral 3 in the drawings which has a solder bump (e.g., 1) provided thereon and the set forth "at least one electrode" can be seen with regard to reference numeral 7 in the drawings, etc.,

although not limited thereto. The set forth "wafer" is shown by 9 reference numeral 9 in the drawings which has semiconductor circuits formed thereon. The example shown in Fig. 20 regarding transistor portion 110 is with regard to a memory cell portion. Similarly, such featured aspects as that covered in claims 1, 3 and 11 are also contained with regard to independent claims 14 and 18, although presented with some modification therefrom.

With regard to new claim 21, the discussion on page 15, line 19, to page 18, line 10, in the present specification is related thereto.

With regard to claim 22, see Figs. 20 and 21 as well as Sketches A and B attached hereto.

With regard to new claim 23, the description on page 21, line 18, to page 22, line 3, in the Specification is related thereto.

With regard to new claims 24 and 25, see the discussion from page 15, line 19, to page 18, line 10, of the specification and, also, Figs. 20-21.

With regard to new claims 26 and 27, see Figs. 20-21.

With regard to new claim 28, see the discussion from page 15, line 19, to page 18, line10, of the specification and, also, Figs. 20-21.

With regard to new claim 29, see the discussion from page 21, line 18, to page 22, line 3, of the specification.

With regard to new claim 30, see the discussion from page 15, line 19, to page 18, line 10, of the specification and, also, Figs. 20-21.

With regard to new claim 31, see Fig. 29.

As to the outstanding objection to the drawings, Applicants accordingly traverse for the following reasons.

It is alleged that the limiting aspects as originally set forth in dependent claims 3 and 11 are not shown in the drawings as is required under 37 C.F.R. §1.83(a). However, in view of the clarifying amendments presented hereinabove, such featured aspects are, in fact, shown in the drawings. With regard to this, amended claim 3 now contains the set forth featured aspects originally included in the now cancelled claim 2 and claim 11 has been re-presented in an appropriate self-contained format. With regard to this, the original limitation in claims 3 and 11 was amended to read instead as follows:

> "the transistor portion is placed in an outer circumferential portion of the surface of the semiconductor device. . . .",

The semiconductor device is now defined as including a transistor portion (e.g., memory cell 110 in Fig. 20). Supportive discussion can be found on page 60, line 11 to page 62, line 2, in the present specification and Figs. 38-39c. According to the description, the transistor portion is specified as "transistor area," and its location in a plane of the semiconductor device is defined such that "the transistor area apt to be affected easily by α-rays is disposed in the outer circumference whereas the area hardly affected by α-rays is disposed in the center and its vicinity of the semiconductor device 13." This location is depicted, for example, in Fig. 39b of the drawings with regard to the arrangements of "areas apt to be affected by α-rays" in contrast to an "area hardly apt to be affected by α-rays." Related discussion regarding this is also provided earlier in these remarks. Comparing Figs. 20 and 21 with Figs. 39a and 39b, it is clearly apparent that the set forth "at least one electrode" (e.g., aluminum pads 7) of the semiconductor element is exemplified as the area that is hardly affected by

α-rays. In view of the above supportive discussion, it is clearly apparent that the questioned limitations in original claims 3 and 11, as presently amended, in independent claims 3 and 11, are fully supported and are also shown in the drawing illustrations. For at least the above reasons, reconsideration and withdrawal of the outstanding objection to the drawings is respectfully requested.

It is submitted since the outstanding objection to the drawings has been rendered moot and noting that claims 3 and 11 were indicated as being otherwise allowable (see item 7 on page 7 of the outstanding Office Action), favorable action therefor on the now-amended claims 3 and 7, both of which were re-presented in an appropriate self-contained format, is respectfully requested.

Claims 1, 2, 5, 8, 9, 12, 14, 15, 18, and 19 stand rejected under 35 U.S.C. §102(e) as anticipated by Shimoishizaka et al. (US Patent 6,313,532); claim 4 stands rejected under 35 U.S.C. §103(a) over the combination of Shimoishizaka et al., as applied to claims 1 and 8, in view of Payne et al. (US Patent 6,057,598); and claims 6, 7, 10,. 13, 16, 17, and 20 stand rejected under 35 U.S.C. §103(a) over the combination of Shimoishizaka et al., supra, in view of Hashimoto (US2002/0024124). As will be shown hereinbelow, the invention according to these claims, as currently amended, and, also, according to the newly-added claims 21-31 could not have been anticipated or suggested in the manner as that alleged in the outstanding rejections. Therefore, insofar as presently applicable, these rejections are traversed and reconsideration and withdrawal of the same is respectfully requested.

Shimoishizaka et al. disclosed a semiconductor device technique which employs a low elasticity layer 20 for absorbing thermal stress and the like caused during heating or cooling of the semiconductor device or to prevent disconnection of metal wires 31. Shimoishizaka et al. technique features a semiconductor device for relaxing stress applied to a connection part thereof (to a mother board) as a result of differences in the thermal expansion coefficient between that of the mother board and the semiconductor device (see col. 2, lines 66, to col. 3, line 7). Shimoishizaka et al. teaches using a lower elasticity layer 20 having a thickness of from 10 to 150 micrometers formed on a semiconductor substrate 10 containing a semiconductor integrated circuit including semiconductor elements such as a transistor (see col. 5, lines 62 to col. 6, line 28, and col. 7, lines 4-12 and Fig. 2).

Shimoishizaka et al., however, failed to disclose or suggest a specific arrangement of semiconductor elements containing the transistor portion in the substrate 10 with reference to the positional placement of the lower elasticity layer 20, etc. Shimoishizaka et al., it is submitted, has also failed to teach controlling the placement of the semiconductor elements and thickness of the insulating layer in consideration of the α-rays concerns, in clear contradistinction with that addressed by the present inventors which led to the present invention, as set forth in the claims 1+, 3+, 11+, 14+ and 18+.

While both Shimoishizaka et al. and the present inventors addressed thermal stress concerns with regard to the semiconductor device technique employed, only the present inventors addressed the α-rays problems arising with regard to the semiconductor device. Also, as to the problem of thermal stress on

semiconductor elements of a semiconductor device, the present inventors, it is submitted, recognized that such problem becomes even more significant with an increase in size of the device. Conversely, if an area of the semiconductor device remains smaller with reference to the mother board (e.g., the circuit substrate), such problem becomes negligible or, practically, disappears.

A main featured aspect of the invention is to provide, in effect, a dead space where a transistor portion (e.g., 110) in Figs. 20, 21, etc. is prohibited from being provided in a surface of the semiconductor device under a circumstance such as shown in attached Sketches A and B as it relates to Fig. 20 and 21 of the drawings, namely, a location underlying the relaxation insulator 5, referred to as Dead Space, having a thickness below the minimum requirements to avoid adverse effects due to α-rays radiation. As can be seen from attached Exhibit A, the dead space (where semiconductor element is not formed) is provided in an area of the surface of the semiconductor device that is still covered with electrically insulating layer 5, but whose thickness is insufficient to block the α-ray radiation which penetrates through the solder bump. However, the dead space provided in an area of the surface must not become so large as to unduly increase the affect due to thermal stress.

Moreover, in consideration of the electrical connection of the external connection terminal (e.g., 3) formed on the electrically insulating layer (e.g., 5) to the electrode (e.g., 7) formed on the surface of the semiconductor device (e.g., 13), exposed from the electrically insulating layer, the dead space necessarily must be wider to permit the electrical connection (e.g., 7) to get over the step portion (incline) of the electrically insulating layer (e.g., 5). In other words, the

aim of the present invention clearly appears to be contrary to the intended result taught Shimoishizaka et al. Namely, the invention as presently set forth is directed to the semiconductor device which is schemed to achieve reduction of the thermal stress in the manufactured semiconductor device (e.g.,13) and prevent, also, α-rays from reaching the transistor portion (e.g., 110). For at least the above reasons, the invention according to amended claims 1+, 3+, 11+, 14+ and 18+ not only could not have been anticipated by or rendered obvious in view Shimoishizaka et al, but, also, could not have been realized even over the combined teachings of Shimoishizaka et al. and Hashimoto and/or Payne et al., such as applied in the standing rejections.

Payne et al. was cited for allegedly teaching a packaged memory cell structure. Also, Hashimoto was cited for its teaching of a polyimide type of insulator, which has low elasticity. However, both Payne et al. and Hashimoto fail to overcome the deficiencies of Shimoishizaka et al.'s teachings, insofar as the present claimed subject matter is concerned. Therefore, for the same and similar reasons as that argued above, the invention could not have been rendered obvious even in view of the combined teachings of Shimoishizaka et al. with Hashimoto and Payne et al.

Therefore, in view of the amendments presented hereinabove together with these accompanying remarks, reconsideration and withdrawal of the outstanding objection and rejections as well as favorable action on all of the presently pending claims, i.e., claims 1 and 3-31,and an early formal notification of allowability of the above-identified application is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 500.39252VX1), and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP

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